

**What is claimed is:**

1. A circuit comprising:
  - an input port and a first output port;
  - a first common-source nFET having a drain-source current and comprising a gate connected to the input port;
  - a first load connected to the first output port;
  - a first current mirror to mirror the drain-source current of the first common-source nFET to the first load;
  - a first common-source pFET having a drain-source current and comprising a gate connected to the input port;
  - a second load connected to the first output port; and
  - a second current mirror to mirror the drain-source current of the first common-source pFET to the second load.
2. The circuit as set forth claim 1, further comprising:
  - a second output port;
  - a second common-source nFET comprising a gate connected to the input port and a drain connected to the second output port; and
  - a second common-source pFET comprising a gate connected to the input port and a drain connected to the second output port.
3. The circuit as set forth in claim 2,

wherein the first load comprises a first common-gate, common-source nFET comprising a gate biased at a reference voltage; and

wherein the second load comprises a first common-gate, common-source pFET comprising a gate biased at the reference voltage.

4. The circuit as set forth in claim 3, the second common-source nFET having a drain-source current and the second common-source pFET having a drain-source current, the circuit further comprising:

a second common-gate, common-source nFET comprising a gate biased at the reference voltage;

a third current mirror to mirror the drain-source current of the second common-source nFET to the second common-gate, common-source nFET;

a second common-gate, common-source pFET comprising a gate biased at the reference voltage; and

a fourth current mirror to mirror the drain-source current of the second common-source pFET to the second common-gate, common-source pFET.

5. The circuit as set forth in claim 4,

wherein the first current mirror has a first gain and the second current mirror has a second gain;

wherein the first common-source nFET has a small-signal transconductance, and the second common-source nFET has a small-signal transconductance equal to the small-signal transconductance of the first common-source nFET scaled by the first gain; and

wherein the first common-source pFET has a small-signal transconductance, and the second common-source pFET has a small-signal transconductance equal to the small-signal transconductance of the first common-source pFET scaled by the second gain; and wherein the circuit loads the first and second output ports with equal small-signal loads.

6. The circuit as set forth in claim 1,

wherein the first load comprises a first common-gate, common-source nFET comprising a gate biased at a reference voltage; and

wherein the second load comprises a first common-gate, common-source pFET comprising a gate biased at the reference voltage.

7. The circuit as set forth in claim 2,

wherein the first current mirror has a first gain and the second current mirror has a second gain;

wherein the first common-source nFET has a small-signal transconductance, and the second common-source nFET has a small-signal transconductance equal to the small-signal transconductance of the first common-source nFET scaled by the first gain; and

wherein the first common-source pFET has a small-signal transconductance, and the second common-source pFET has a small-signal transconductance equal to the small-signal transconductance of the first common-source pFET scaled by the second gain; and

wherein the circuit loads the first and second output ports with equal small-signal loads.

8. A circuit comprising:
- an input port and a first output port;
  - a first common-source nFET comprising a gate connected to the input port and comprising a drain;
  - a first current mirror comprising a first port connected to the drain of the first common-source nFET and comprising a second port;
  - a first common-gate, common-source nFET comprising a drain connected to the second port of the first current mirror and to the first output port, and comprising a gate biased at a reference voltage;
  - a first common-source pFET comprising a gate connected to the input port and comprising a drain;
  - a second current mirror comprising a first port connected to the drain of the first common-source pFET and comprising a second port; and
  - a first common-gate, common-source pFET comprising a drain connected to the second port of the second current mirror and to the first output port, and comprising a gate biased at the reference voltage.
9. The circuit as set forth in claim 8, further comprising:
- a second output port;
  - a second common-source nFET comprising a gate connected to the input port and comprising a drain connected to the second output port;

a third current mirror comprising a first port connected to the drain of the second common-source nFET and comprising a second port;

a second common-gate, common-source nFET comprising a drain connected to the second port of the third current mirror and comprising a gate biased at the reference voltage;

a second common-source pFET comprising a gate connected to the input port and comprising a drain connected to the second output port;

a fourth current mirror comprising a first port connected to the drain of the second common-source pFET and comprising a second port; and

a second common-gate, common-source pFET comprising a drain connected to the second port of the fourth current mirror and comprising a gate biased at the reference voltage.

10. The circuit as set forth in claim 9,

wherein the first current mirror has a first gain and the second current mirror has a second gain;

wherein the first common-source nFET has a small-signal transconductance, and the second common-source nFET has a small-signal transconductance equal to the small-signal transconductance of the first common-source nFET scaled by the first gain; and

wherein the first common-source pFET has a small-signal transconductance, and the second common-source pFET has a small-signal transconductance equal to the small-signal transconductance of the first common-source pFET scaled by the second gain; and

wherein the first current mirror and the first common-gate, common-source nFET loads the first output port with a first small-signal load, and the second common-source nFET and the third current mirror load the second output port with a small-signal load equal to the first small-signal load; and

wherein the second current mirror and the first common-gate, common-source pFET loads the first output port with a second small-signal load, and the second common-source pFET and the fourth current mirror load the second output port with a small-signal load equal to the second small-signal load.

11. A circuit comprising:

an input port and a first output port;

a first common-source nFET comprising a gate connected to the input port and comprising a drain;

a first pFET comprising a drain connected to the drain of the first common-source nFET and comprising a gate connected to the drain of the first pFET;

a second pFET comprising a gate connected to the gate of the first pFET and comprising a drain;

a first common-source, common-gate nFET comprising a drain connected to the drain of the second pFET and to the first output port, and comprising a gate biased at a reference voltage;

a first common-source pFET comprising a gate connected to the input port and comprising a drain;

a first nFET comprising a drain connected to the drain of the first common-source nFET and comprising a gate connected to the drain of the first nFET;

a second nFET comprising a gate connected to the gate of the first nFET and comprising a drain; and

a first common-source, common-gate pFET comprising a drain connected to the drain of the second nFET and to the first output port, and comprising a gate biased at the reference voltage.

12. The circuit as set forth in claim 11, further comprising:

a second output port;

a second common-source nFET comprising a gate connected to the input port and comprising a drain connected to the second output port;

a third pFET comprising a gate and a drain connected to the drain of the second common-source nFET;

a fourth pFET comprising a gate connected to the gate of the third pFET and comprising a drain connected to the gate of the fourth pFET;

a second common-source, common-gate nFET comprising a drain connected to the drain of the fourth pFET and comprising a gate biased at the reference voltage;

a second common-source pFET comprising a gate connected to the input port and comprising a drain connected to the second output port;

a third nFET comprising a gate and a drain connected to the drain of the second common-source pFET;

a fourth nFET comprising a gate connected to the gate of the third nFET and comprising a drain connected to the gate of the fourth nFET; and

a second common-source, common-gate pFET comprising a drain connected to the drain of the fourth nFET and comprising a gate biased at the reference voltage.

13. The circuit as set forth in claim 12,

wherein the first common-source nFET, the second common-source nFET, the first pFET, and the second pFET each have a small-signal transconductance such that the product of the second common-source nFET small-signal transconductance with the first pFET small-signal transconductance is equal to the product of the first common-source nFET small-signal transconductance with the second pFET small-signal transconductance; and

wherein the first common-source pFET, the second common-source pFET, the first nFET, and the second nFET each have a small-signal transconductance such that the product of the second common-source pFET small-signal transconductance with the first nFET small-signal transconductance is equal to the product of the first common-source pFET small-signal transconductance with the second nFET small-signal transconductance.

14. The circuit as set forth in claim 13,

wherein the second pFET, the first common-source, common-gate nFET, the third pFET and the second common-source nFET each have a small-signal drain-source resistance such that the parallel combination of the small-signal drain-source resistances

for the second pFET and the first common-source, common-gate nFET is equal to the parallel combination of the small-signal drain-source resistances for the third pFET and the second common-source nFET; and

wherein the second nFET, the first common-source, common-gate pFET, the third nFET and the second common-source pFET each have a small-signal drain-source resistance such that the parallel combination of the small-signal drain-source resistances for the second nFET and the first common-source, common-gate pFET is equal to the parallel combination of the small-signal drain-source resistances for the third nFET and the second common-source pFET.

15. A computer system comprising a first die and a second die in communication with the first die, the second die comprising a circuit comprising:

an input port and a first output port;

a first common-source nFET having a drain-source current and comprising a gate connected to the input port;

a first load connected to the first output port;

a first current mirror to mirror the drain-source current of the first common-source nFET to the first load;

a first common-source pFET having a drain-source current and comprising a gate connected to the input port;

a second load connected to the first output port; and

a second current mirror to mirror the drain-source current of the first common-source pFET to the second load.

16. The computer system as set forth claim 15, the circuit further comprising:  
a second output port;  
a second common-source nFET comprising a gate connected to the input port and  
a drain connected to the second output port; and  
a second common-source pFET comprising a gate connected to the input port and  
a drain connected to the second output port.

17. The computer system as set forth in claim 16,  
wherein the first load comprises a first common-gate, common-source nFET  
comprising a gate biased at a reference voltage; and  
wherein the second load comprises a first common-gate, common-source pFET  
comprising a gate biased at the reference voltage.

18. The computer system as set forth in claim 17, the second common-source nFET  
having a drain-source current and the second common-source pFET having a drain-  
source current, the circuit further comprising:

a second common-gate, common-source nFET comprising a gate biased at the  
reference voltage;

a third current mirror to mirror the drain-source current of the second common-  
source nFET to the second common-gate, common-source nFET;

a second common-gate, common-source pFET comprising a gate biased at the  
reference voltage; and

a fourth current mirror to mirror the drain-source current of the second common-source pFET to the second common-gate, common-source pFET.

19. The computer system as set forth in claim 18,

wherein the first current mirror has a first gain and the second current mirror has a second gain;

wherein the first common-source nFET has a small-signal transconductance, and the second common-source nFET has a small-signal transconductance equal to the small-signal transconductance of the first common-source nFET scaled by the first gain; and

wherein the first common-source pFET has a small-signal transconductance, and the second common-source pFET has a small-signal transconductance equal to the small-signal transconductance of the first common-source pFET scaled by the second gain; and

wherein the circuit loads the first and second output ports with equal small-signal loads.

20. The computer system as set forth in claim 15,

wherein the first load comprises a first common-gate, common-source nFET comprising a gate biased at a reference voltage; and

wherein the second load comprises a first common-gate, common-source pFET comprising a gate biased at the reference voltage.